

Notice of References Cited	Application/Control No. 09/531,633	Applicant(s)/Patent Under Reexamination LI, ZHE	
	Examiner Eduardo Garcia-Otero	Art Unit 2123	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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	C	US-5,642,304	06-1997	Simpson, John Richard	708/446
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	L	US-			
	M	US-			

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"Logic Verification using Binary Decision Diagrams in a Logic Synthesis Environment" by Sharad Malik et al., 1988 IEEE, pages 6-9.
	V	"Boolean Functions Classification via Fixed Polarity Reed-Muller Forms" by Chien-Chung Tsai et al., 1997 IEEE TRANSACTIONS ON COMPUTERS, Vol 46, No. 2, pages 173-186.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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